REMARKS

Status of the Claims

Applicants request the Examiner to reconsider the application as amended. Claims 1-16 are pending. Claims 17-32 have been canceled. Claims 6-7, 9, 11, and 13-15 have been objected to as being dependant upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. (Final Office Action, page 3). Applicants wish to express appreciation to the Examiner for the indication of allowable subject matter.

Claim 1 has been amended to recite "wherein the thinning process comprises at least one etching process." Support for this amendment can, for example, be found in the originally filed specification page 5, second paragraph; page 8, first paragraph; Examples 1-3; and claims 8-11.

Rejection of Claims 1-5, 8, 10, 12, and 16 Under 35 U.S.C. § 102(a) in view of Mitsuhashi

In an Advisory Action dated January 19, 2006, a final rejection of claims 1-5, 8, 10, 12, and 16 under 35 U.S.C. § 102(a) was maintained in view of U.S. Published Application No. 2003/0104706 to Mitsuhashi et al. ("Mitsuhashi"). In view of the Advisory Action and the reasoning set forth therein (*see* Advisory Action, page 2), Applicants draw the Examiner's attention to amended claim 1 which recites:

> A method for making an ultrathin high-k gate dielectric for use in a field effect transistor comprising:
>
> depositing a high-k gate dielectric material on a substrate;
>
> forming an ultrathin high-k dielectric by performing a thinning process on said high-k gate dielectric material, wherein the ultrathin high-k dielectric

has a thickness of less than about 3 nm; and, ***following the thinning process,***

forming a conductive gate structure on said ultrathin high-k dielectric;

wherein the thinning process comprises at least one etching process.

(emphasis added). Applicants submit that this amended claim is patentable over Mituhashi.

Specifically, Applicants submit that Mitsuhashi does not teach a thinning process on a high-k dielectric, wherein the thinning process comprises at least one etching process, and then, following this thinning process, forming a conductive gate structure on the ultrathin high-k dielectric. Instead, Mitsuhashi teaches forming a gate electrode structure ***prior to*** performing any etching process. *See, e.g.*, Mitsuhashi, page 2, paragraph [0022] ("a third step of patterning the conductive film so as to form a gate electrode . . . a fifth step of removing, by wet-etching, the exposed portion of the metal oxide film . . ."). Indeed, nowhere does Mitsuhashi teach or suggest performing an etching step of high-k dielectric material and then forming a conductive gate electrode. Instead, the reference consistently teaches the opposite — forming a gate electrode prior to any disclosed etching step. *See, e.g.*, Mitsuhashi, page 5, paragraphs [0056] to [0062]; page 77, paragraphs [0077] to [0080]; *see also* Mitsuhashi claim 6. Therefore, for at least this reason, Mitsuhashi fails to teach or suggest the method recited in amended claim 1.

Accordingly, applicants submit that claims 1-16 are in immediate condition for allowance.

Conclusion

In view of the foregoing, the rejections should be withdrawn and all pending claims should be allowed.

If prosecution may be further advanced, Examiner is invited to telephone the undersigned to discuss this application.

Applicants believe no fees are due in conjunction with the filing of this Amendment. However, if any additional fees are due, such as a fee for a further extension of time, please charge the fees to Deposit Account No. 50-0510.

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Respectfully submitted,

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